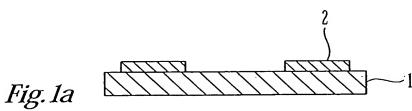
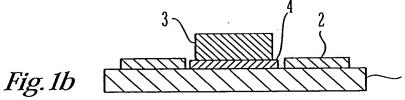
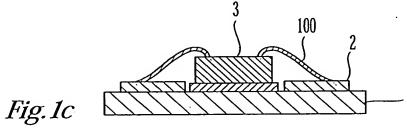
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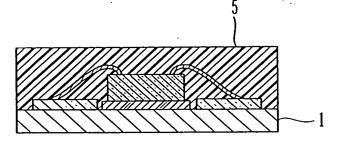


Fig.1d

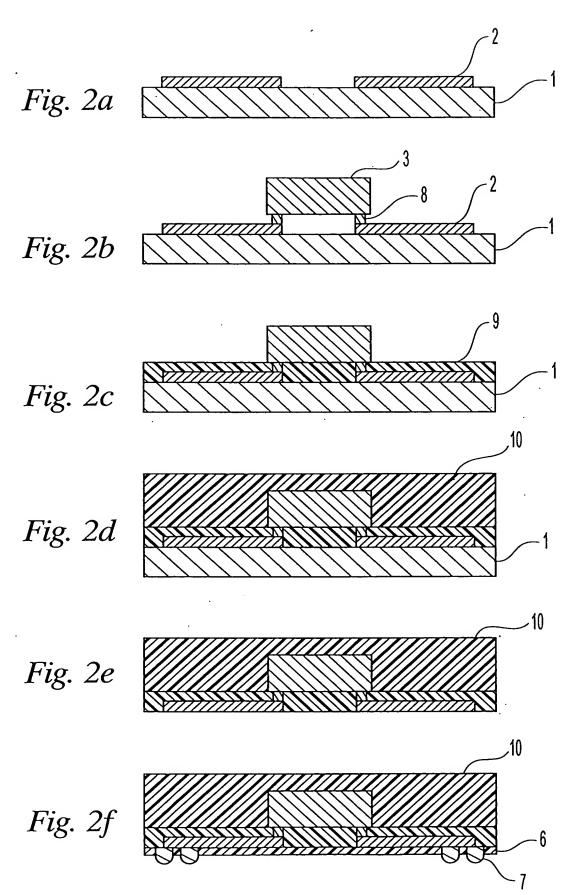


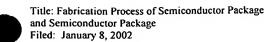
Fig. 1e

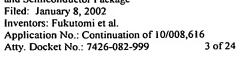


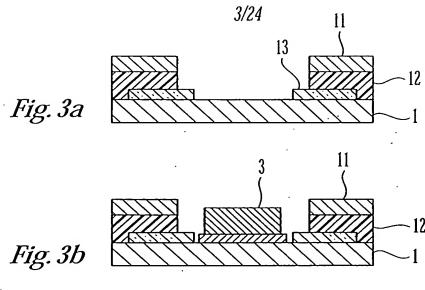
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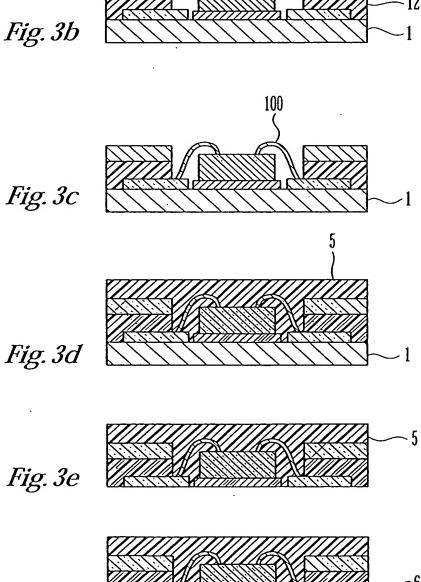
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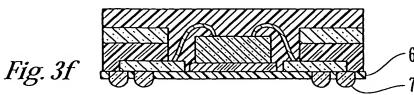






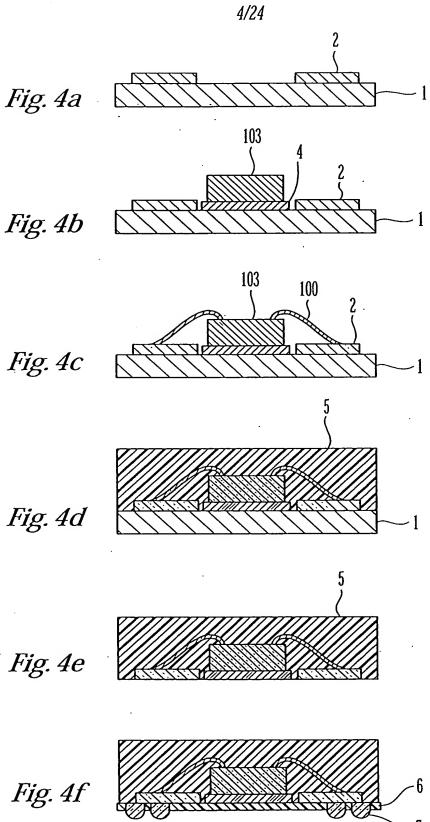






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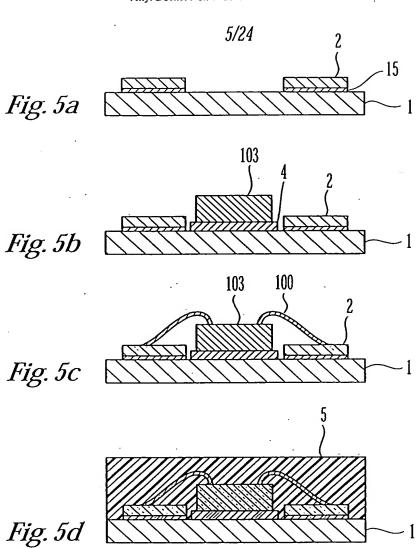


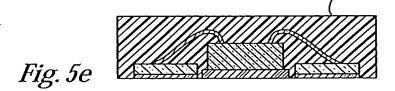
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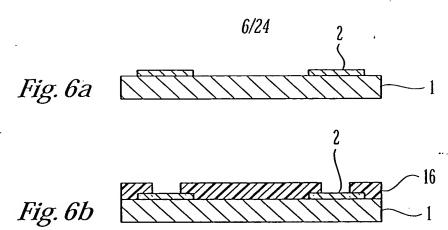


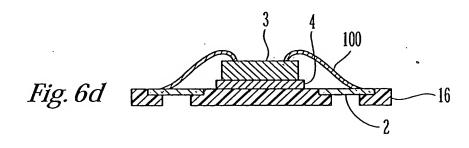


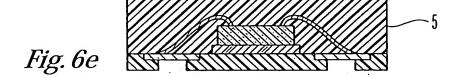


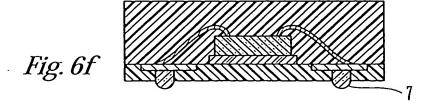
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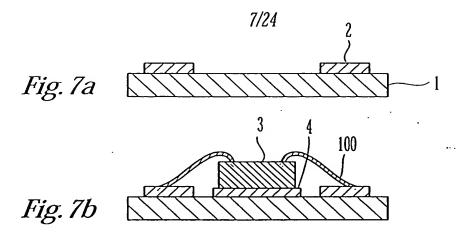


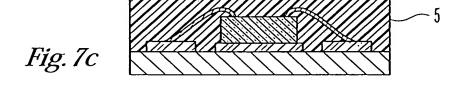




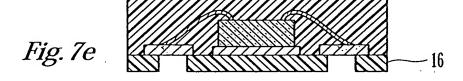
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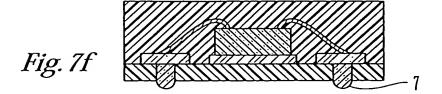
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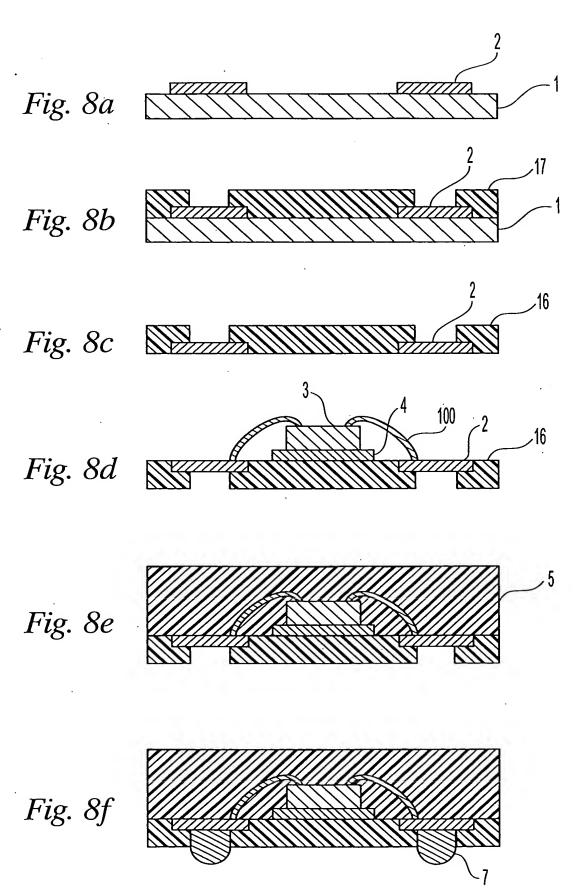






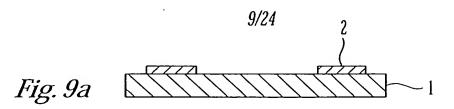
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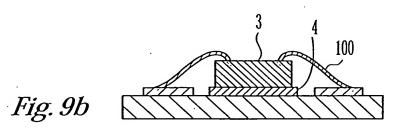
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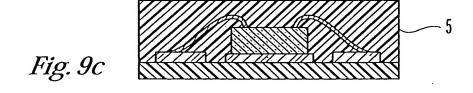


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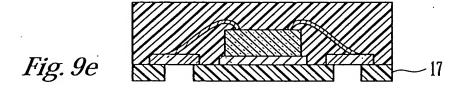
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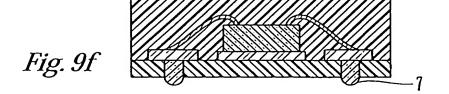












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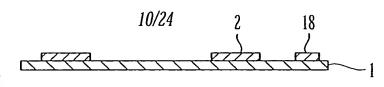
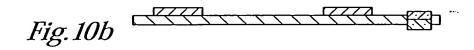
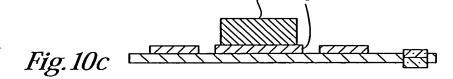
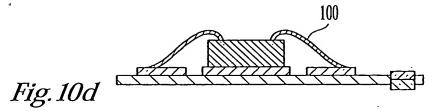
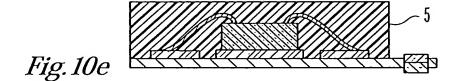


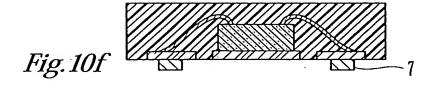
Fig. 10a

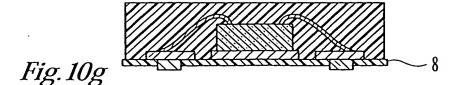












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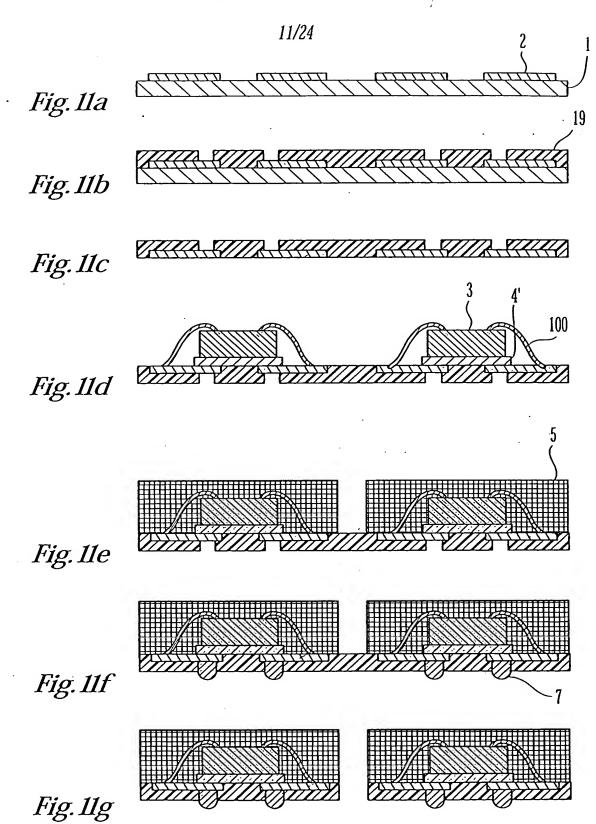
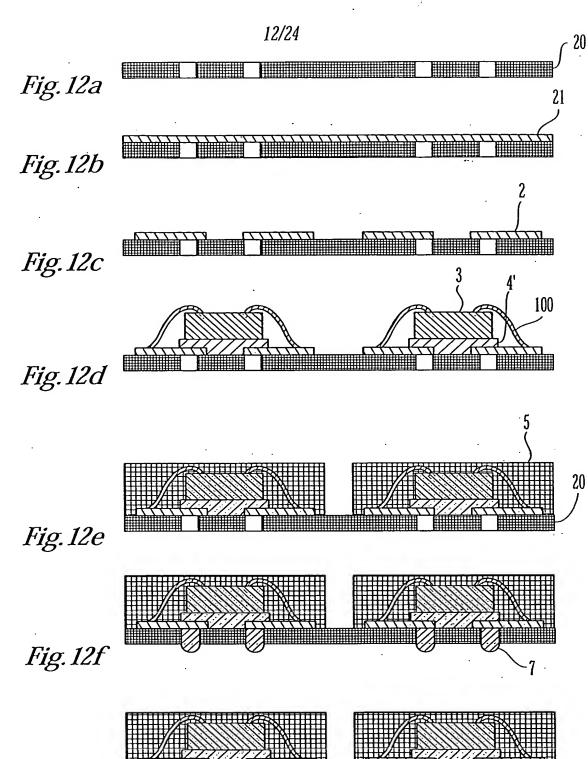


Fig. 12g

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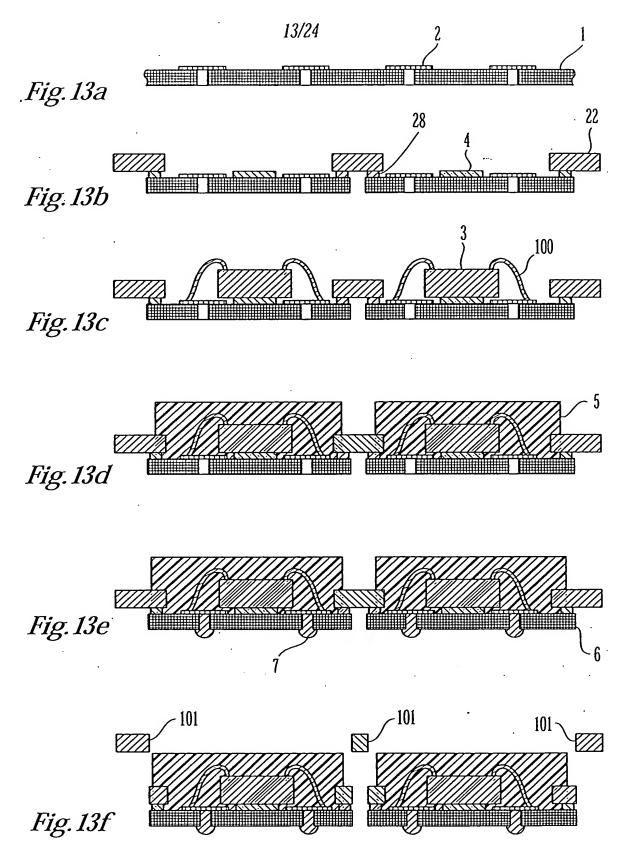
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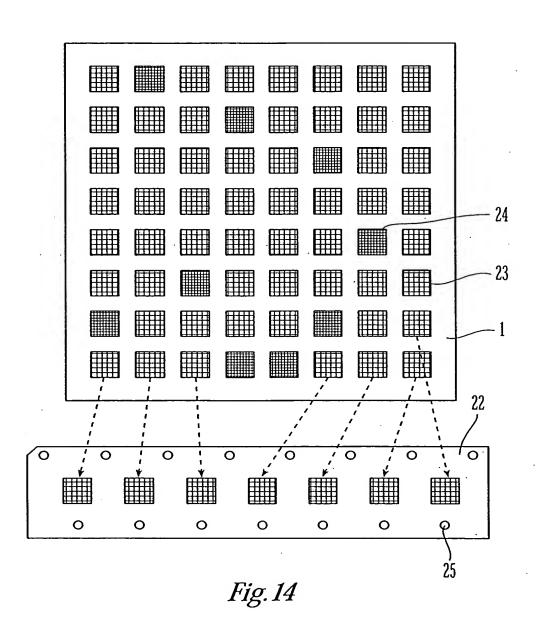
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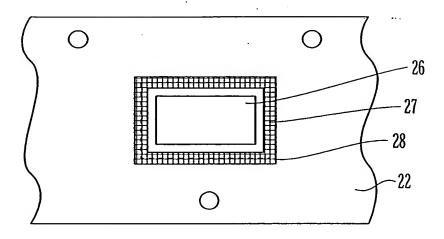


Fig. 15a

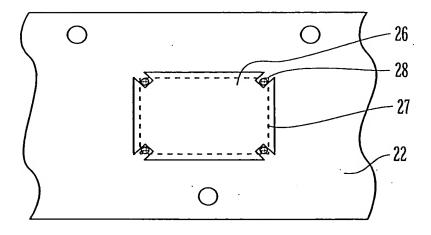
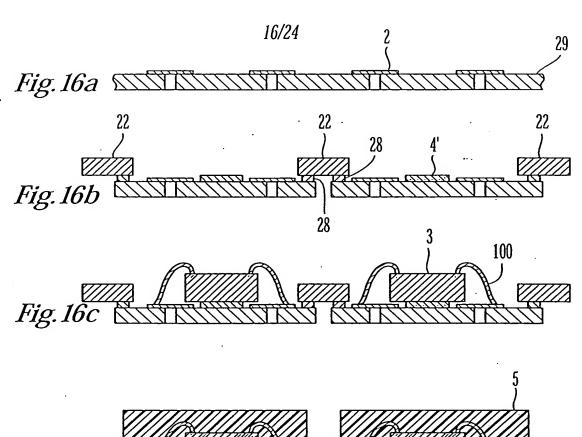
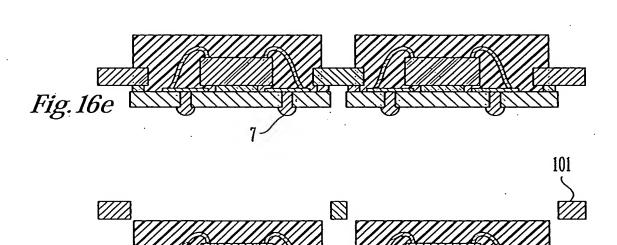


Fig. 15b

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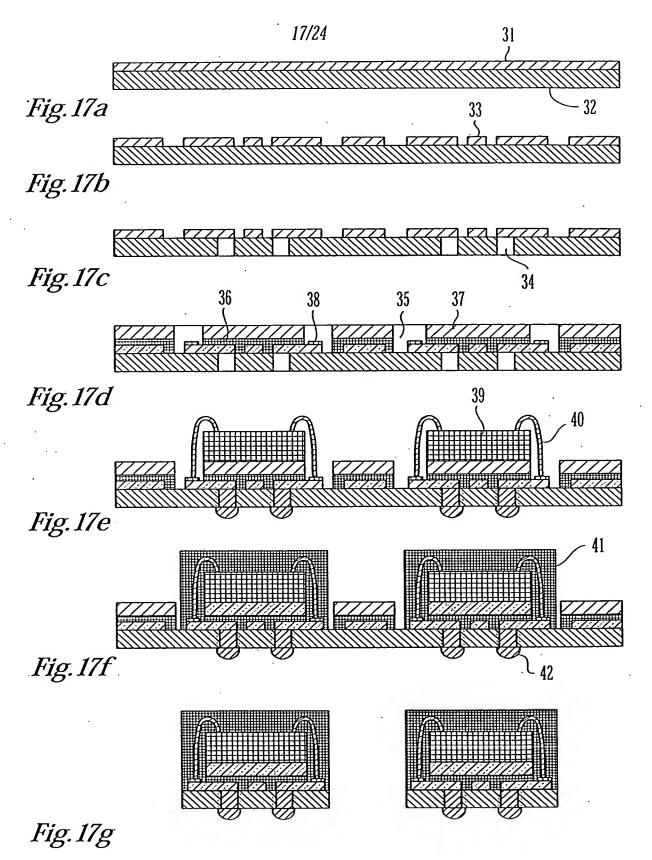
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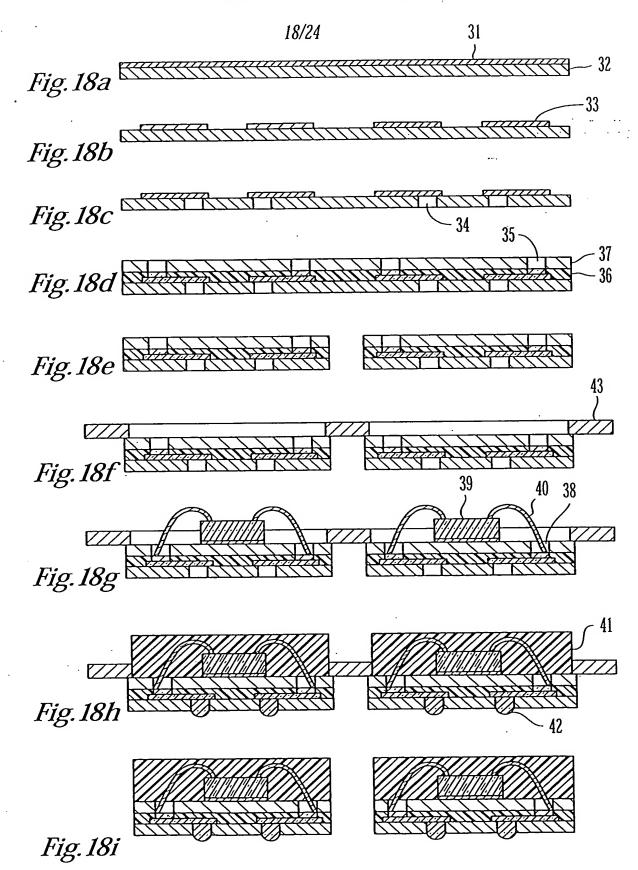
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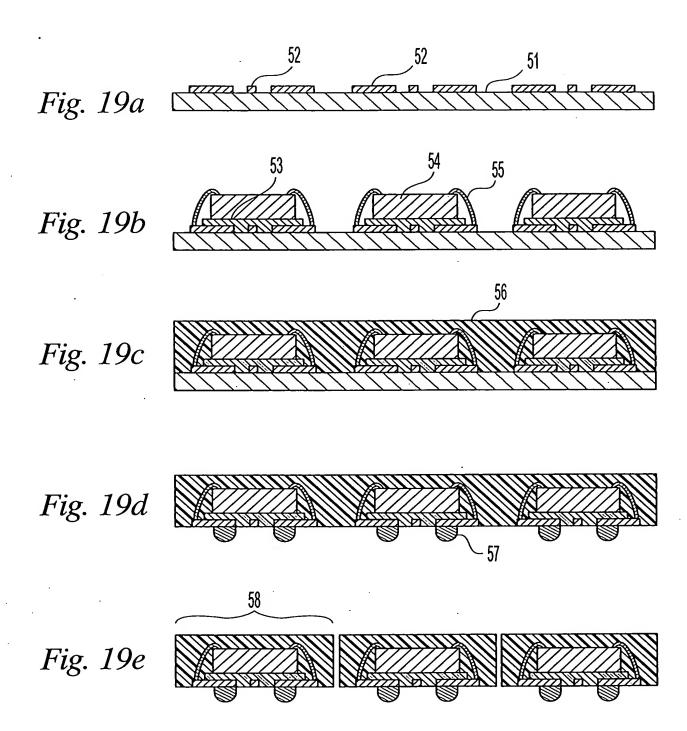
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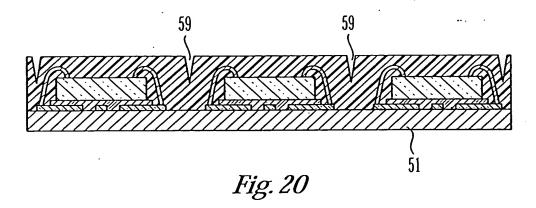


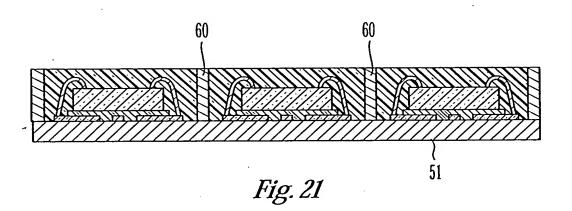
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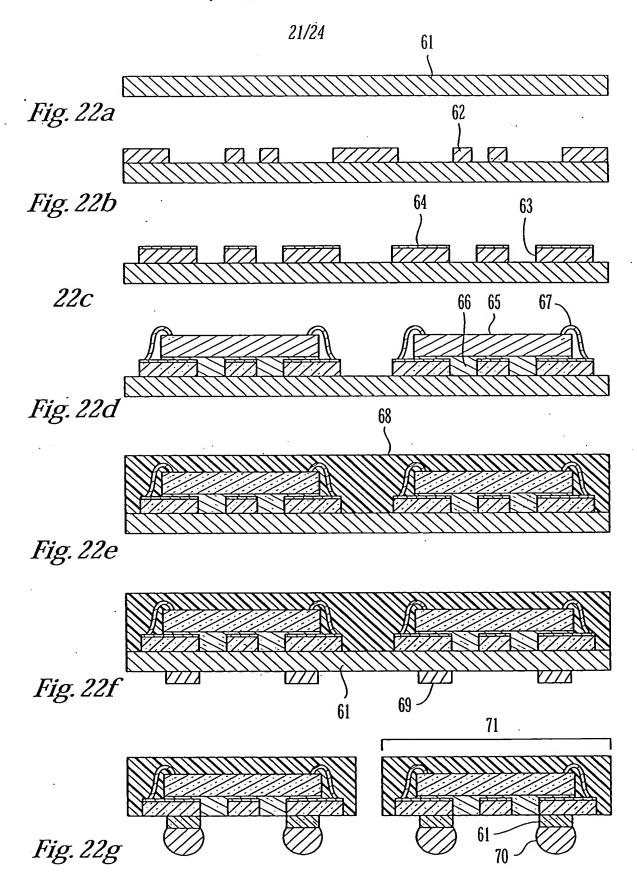
Title: Fabrication Process of Semiconductor Package and Semiconductor Package
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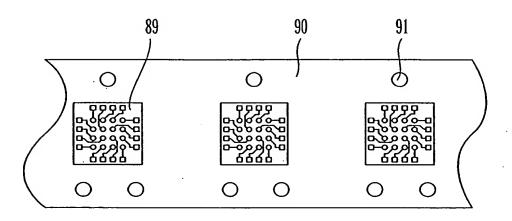
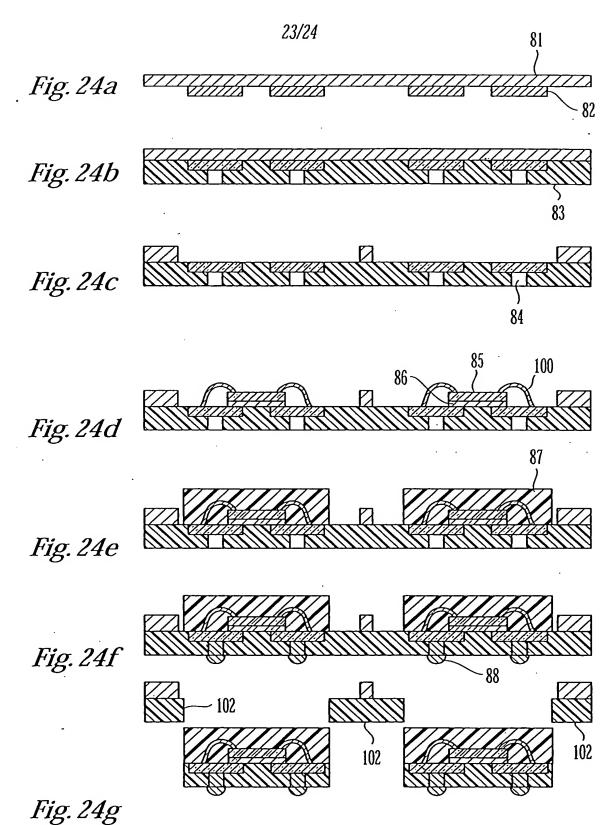


Fig. 23

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